01-31-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Eric T. Stubbs
Title: VARIABLE DELAY LINE
Attorney Docket No.: 303.662US1

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VARIABLE DELAY LINE

Technical Field of the Invention

The present invention relates generally to delay elements, and in particular, the present invention relates to variable delay lines used in delay lock loops.

Background of the Invention

Electronic systems typically include circuit boards, and the circuit boards typically include semiconductor devices. Some semiconductor devices communicate with each other using clock signals for timing. For example, devices using a common clock signal can communicate with one another by driving data when sending, and latching data when receiving, using timing derived from the common clock signal.

Clock signals can be used to control timing internal to the semiconductor devices, and can also be used to control timing external to the semiconductor devices. For example, in devices having internal storage elements, or "synchronous" elements, an internal clock signal is "fanned out" to the synchronous elements internal to the device such that the internal synchronous elements can reliably communicate. These semiconductor devices can also drive data from within the device through conductors at the device boundary, and drive signal nodes external to the device.

When a clock signal is received by a semiconductor device, it undergoes a finite amount of delay when entering the device. This delay can be caused by trace impedance, input driver delay, or the like. The clock signal on the semiconductor die is, therefore, delayed with respect to the clock outside the device. When one clock signal has undergone a delay different from another clock signal, the two clock signals are said to have a phase offset. When the clock signal internal to the device has a phase offset relative to a clock signal outside the device, timing from one device to another can be upset, thereby causing errors when the devices are communicating.

Delay lock loops have been devised to add additional clock delay to the clock signal such that the total delay is substantially equal to an integer number of clock

periods. If the total delay is an integer number of clock periods, the phase offset is zero. When a device is powered on, or when the device is reset, the delay lock loop begins to operate. Delay lock loops typically add or subtract a unit delay element from the internal clock path each clock period until a desired phase offset between the internal and external clock signals is reached. This can be time consuming, especially if the initial phase offset is large, or if the clock frequency is low.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate methods and apparatus for controlling phase offsets between clock signals.

Summary of the Invention

The above mentioned problems and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

In one embodiment, a method of setting a delay value in a delay lock loop includes delaying a first signal in a variable delay line to generate a second signal, and comparing a phase of the first signal with a phase of the second signal to generate a first control signal. The method further includes delaying the first signal by a first substantially fixed amount to generate a third signal, and comparing the phase of the second signal with a phase of the third signal to generate a second control signal. Responsive to the first control signal the variable delay line is adjusted by a first delay amount, and responsive to the second control signal the variable delay line is adjusted by a second delay amount.

In another embodiment, an integrated circuit includes a variable delay line having an input node, an output node, a fine adjustment node, and a coarse adjustment node. The integrated circuit further includes a phase detector configured to compare a signal on the input node with a signal on the output node and drive signals onto the fine adjustment node and the coarse adjustment node.

Brief Description of the Drawings

Figure 1 is an integrated circuit that includes a delay lock loop of the present invention.

Figure 2 is a phase detector of the present invention.

Figure 3 is a variable delay line of the present invention.

Figure 4 is a shift register having coarse and fine control in accordance with the present invention.

Figure 5 is an alternate embodiment of a variable delay line of the present invention.

Figure 6 shows waveforms during the operation of a variable delay line.

Figure 7 shows a processing system according to the invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 1 shows an integrated circuit having a delay lock loop. Integrated circuit 100 includes input buffer 106, device element 112, and a delay lock loop. The delay lock loop includes variable delay line 108, phase detector 130, device element delay model 116, and delay element 120.

Integrated circuit 100 receives an external clock into input buffer 106 on input node 102. Input buffer 106 is at the device boundary, and inserts a "device boundary

delay" in the signal on input node 102. A device boundary delay can be introduced by mechanisms other than input buffer 106. For example, a delay line can insert a device boundary delay. Input buffer 106 receives the external clock signal into integrated circuit 100, and provides a delayed version of the external clock to variable delay line 108 and phase detector 130 on node 104. For the purpose of description, the clock signal on node 104 is referred to herein as "E_CLOCK." E_CLOCK is delayed from the external clock on node 102, by an amount equal to the device boundary delay introduced by input buffer 106.

Variable delay line 108 receives E_CLOCK on node 104, and subjects E_CLOCK to further delay to generate the internal clock on node 110. The internal clock on node 110 is used internal to integrated circuit 100. In some embodiments, such as the embodiment shown in Figure 1, the internal clock is fanned out to device elements within the integrated circuit. Device element 112 is representative of many possible device elements within integrated circuit 100, and can be any type of circuit element that uses the internal clock. Examples include, but are not limited to, flip-flops, latches, output registers, and output buffers. Device element 112 receives the internal clock on control input node 114. Control input node 114 can be a clock input, an output enable input, a data input, or the like. For example, in some embodiments, device element 112 is a flip-flop and control input node 114 is a clock input. In other embodiments, device element 112 is a buffer and control input node 114 is an output enable that switches an output from a high impedance state to a driven state.

The internal clock on node 110 is also fed back through device element delay model 116 and delay element 120 to phase detector 130. Device element delay model 116 has a delay characteristic that closely matches that of device element 112, and delay element 120 has a delay characteristic that closely matches that of input buffer 106. The delayed clock signal on node 122 is referred to herein as "I_CLOCK."

Phase detector 130 compares the phase of I_CLOCK to the phase of E_CLOCK and controls the delay of variable delay line 108. In the embodiment of Figure 1, phase detector 130 generates a fine adjustment control on node 132 and a coarse adjustment control on node 134. When the phase offset between E_CLOCK and I_CLOCK is

large, the coarse adjustment control can make large adjustments to the delay of variable delay line 108, and when the phase offset is small, the fine adjustment control can make smaller adjustments. Node 132 and node 134 can include multiple signal lines. For example, node 132 may include more than one signal line, and node 134 may include more than one signal line. The operation of phase detector 130 and variable delay line 108 is described in greater detail with reference to the remaining figures.

In some embodiments, when variable delay line 108 is in steady state, the sum of the delay in variable delay line 108, device element delay model 116, and delay element 120 is an integer number of clock periods. When the sum of the delay is an integer number of clock periods, E_CLOCK and I_CLOCK substantially align in phase, and phase detector 130 does not make adjustments.

In the embodiment shown in Figure 1, when E_CLOCK and I_CLOCK are substantially aligned in phase, the internal clock on node 110 leads the external clock on node 102 by a delay substantially equal to that of device element delay model 116. This can be useful when, for example, device element 112 drives data signals or control signals off integrated circuit 100. In embodiments where device element 112 is an output register and control input node 114 is a clock input, device element delay model 116 can model the clock-to-output delay of the output register. Device element delay model 116 can also exhibit a delay that is more or less than the clock-to-output delay of the output register. This can be useful for generating specific timing relationships between the external clock and the signal driven external to integrated circuit 100.

In some embodiments, device element delay model 116 is omitted. In some of these embodiments, device element 112 is a synchronous device such as a flip-flop that drives data internal to integrated circuit 100. In other embodiments, integrated circuit 100 includes multiple delay lock loops for supplying clock signals to different portions of integrated circuit 100. For example, multiple device elements 112 of different types can exist within integrated circuit 100. When different device elements 112 exhibit different delays, multiple delay lock loops can be utilized to supply internal clock signals with desired phase relationships.

Integrated circuit 100 can be any type of integrated circuit capable of utilizing a delay lock loop. In some embodiments, integrated circuit 100 is a memory device. In some of these embodiments, delay element 112 is a synchronous output element. In others of these embodiments delay element 112 is an asynchronous output element. In other embodiments, integrated circuit 100 is an application-specific integrated circuit (ASIC). In still other embodiments, integrated circuit 100 is a processor, such as a microprocessor, digital signal processor, or the like.

The embodiment shown in Figure 1 provides a mechanism that adjusts a variable delay quickly. Coarse adjustments can be made when phase offsets are large, and fine adjustments can be made when phase offsets are large. When integrated circuit 100 can benefit from a delay lock loop that locks quickly, in part because a substantially fixed relationship between multiple clock signals can be achieved quickly.

Figure 2 shows phase detector 130. Phase detector 130 includes phase comparators 220, 230, and 240. Phase detector 130 also includes delay element 206 and delay element 208. Phase detector 130 receives E_CLOCK on node 202 and I_CLOCK on node 204. Phase comparator 220 generates a fine increase signal on node 222, and a fine decrease signal on node 224. Phase comparator 230 generates a coarse increase signal on node 232, and phase comparator 240 generates a coarse decrease signal on node 242.

Phase comparator 240 compares I_CLOCK on node 204 with a delayed E_CLOCK on node 212. When the phase of I_CLOCK lags the phase of the delayed E_CLOCK, the coarse decrease signal is asserted on node 242. Stated differently, when the phase of I_CLOCK lags the phase of E_CLOCK by an amount greater than the delay of delay element 208, phase comparator 240 asserts the coarse decrease signal on node 242. Phase comparator 230 operates in a manner similar to phase comparator 240, with the exception that I_CLOCK is delayed rather than E_CLOCK. When the phase of the delayed I_CLOCK on node 210 lags the phase of E_CLOCK, phase comparator 230 asserts the coarse increase signal on node 232. Stated differently, when the phase of I_CLOCK lags the phase of E_CLOCK by an amount greater than the delay of delay element 206, phase comparator 230 asserts the coarse increase signal on node 232.

In the embodiment shown in Figure 2, the coarse increase signal on node 232 and the coarse decrease signal on node 242 can be used to make coarse adjustments in a variable delay line, such as variable delay line 108 (Figure 1). In some embodiments, delay elements 206 and 208 have delay values substantially equal to the coarse delay increments controlled by the coarse increase signal and the coarse decrease signal. For example, when phase comparators 230 and 240 are used for coarse adjustment of a variable delay line such as variable delay line 108, the variable delay line can increase the delay by an amount substantially equal to the delay of delay element 206 when the coarse increase signal is asserted. As a result, I_CLOCK is retarded relative to E_CLOCK by an amount substantially equal to the delay of delay element 206. Likewise, the coarse decrease signal can cause a decrease in delay substantially equal to the delay of delay element 208. As a result, I_CLOCK is advanced with respect to E_CLOCK by an amount substantially equal to the delay of delay element 208.

If I_CLOCK lags E_CLOCK less than the delay of delay element 206, the coarse increase signal on node 232 is not asserted. Likewise, if E_CLOCK lags I_CLOCK less than the delay of delay element 208, coarse decrease signal on node 242 is not asserted. Delay element 206 and 208 determine a phase offset window, such that when the phase offset between E_CLOCK and I_CLOCK is within the phase offset window, the coarse adjustment control signals are not asserted.

Phase comparator 220 compares E_CLOCK and I_CLOCK directly. When I_CLOCK lags E_CLOCK more than a fine threshold, the fine increase signal on node 222 is asserted. Likewise, when I_CLOCK lags E_CLOCK more than a fine threshold, the fine decrease signal on node 224 is asserted. The fine increase signal on node 222 and the fine decrease signal on node 224 can be used as fine adjustment control signals on a variable delay line such as variable delay line 108 (Figure 1). When the fine increase signal on node 222 is asserted, the delay of variable delay line 108 is increased, which causes I_CLOCK on node 204 to retard slightly. In contrast, when the fine decrease signal on node 224 is asserted, the variable delay of variable delay line 108 is decreased, which causes I_CLOCK on node 204 to advance slightly.

The embodiment shown in Figure 2 includes three phase comparators. In some embodiments, more than three phase comparators are used. For example, multiple coarse increase signals can be generated using multiple phase comparators, each being coupled to a different delay element corresponding to delay element 206. Also, multiple coarse decrease signals can be generated using multiple phase comparators, each being coupled to a different delay element corresponding to delay element 208. In these embodiments, greater control of a variable delay line can be exercised.

Comparators 230 and 240 in the embodiment shown in Figure 2 compare the phase of two signals after a delay has been introduced. In other embodiments, phase comparators compare the phase of two signals directly and produce a signal having a phase offset value. The phase offset value is then compared to phase offset thresholds to generate coarse and fine adjustment control signals. For example, the phase offset value can be compared to a fine threshold and a coarse threshold. When the phase offset value is larger than the coarse threshold, one of the coarse adjustment control signals can be asserted. When the phase offset value is larger than the fine threshold, but not larger than the coarse threshold, one of the fine adjustment control signals can be asserted, and when the phase offset value is less than the fine threshold, the adjustment control signals can remain de-asserted.

Figure 3 shows variable delay line 108A. Variable delay line 108A is one embodiment of variable delay line 108 (Figure 1). Variable delay line 108A includes multiple delay cells shown in Figure 3 as delay cells 304, 308, 312, and 316. Four delay cells are shown in variable delay line 108A; however, any number of delay cells can be utilized without departing from the scope of the present invention.

Variable delay line 108A also includes shift register 330. Shift register 330 has, as control inputs, a fine increase signal on node 332, a fine decrease signal on node 334, a coarse increase signal on node 336, and a coarse decrease signal on node 338. These control inputs correspond to the fine adjustment controls and coarse adjustment controls as shown in Figure 2.

Shift register 330 includes multiple storage elements such as flip-flops, latches, or the like, each having a control signal output. Each storage element within shift

register 330 holds a single bit in the shift register, and the state of the bit is reflected on the control signal output. The control signal outputs from shift register 330 include control signals on nodes 320, 322, 324, and 326. When a control signal output is asserted, the corresponding delay cell routes the non-E_CLOCK input to the output. For example, when the control signal on node 326 is not asserted, delay cell 316 routes E_CLOCK to node 318. This corresponds to the shortest delay in variable delay line 108A. In contrast, when the control signal on node 326 is asserted, delay cell 316 routes the signal from node 314 to node 318. In this case, the delay of at least delay cell 312 is added to the delay of delay cell 316.

Variable delay line 108A achieves variable delay by routing E_CLOCK through a variable number of delay cells, each having a "unit" delay, to produce the internal clock on node 318. The shortest delay is achieved by routing E_CLOCK through only delay cell 316. Increasing amounts of delay are achieved by adding additional delay cells to delay cell 316. For example, when delay element 312 is cascaded with delay cell 316, the delay in variable delay line 108A is increased. Additional delay cells are added when shift register 330 is "shifted left." When shift register 330 is shifted left, additional control signal outputs are asserted, and additional delay is added to variable delay line 108A.

In some embodiments, shift register 330 can be shifted by more than one storage element to create a coarse increment in the delay of variable delay line 108A. In the embodiment of Figure 3, the coarse increase signal causes a shift left of more than one storage element, and the coarse decrease signal causes a shift right of more than one storage element within shift register 330. In other embodiments, multiple coarse increase and coarse decrease signals are used, each causing shifts of different amounts. The fine increase signal and fine decrease signal cause shifts smaller than the shifts caused by the coarse adjustment signals. In some embodiments, the fine adjustment signals cause shifts of one storage element at a time.

Figure 4 shows shift register 330. Shift register 330 includes storage elements arranged in blocks 410 and 440. Block 410 includes four storage elements corresponding to output nodes 412, 414, 416, and 418. Likewise block 440 includes

four storage elements corresponding to output nodes 442, 444, 446, and 448. Block 410 receives a fine increase signal from node 470 on shift left input node 424, and block 440 receives the fine increase signal on shift left input node 454. Block 410 receives a fine decrease signal from node 472 on shift right input node 426, and block 440 receives the fine decrease signal on shift right input node 456. When the fine increase signal is asserted, blocks 410 and 440 perform a shift left operation. Likewise, when the fine decrease signal is asserted, blocks 410 and 440 perform a shift right operation.

The shift left and shift right operations perform a shift of a single bit. For example, if the storage elements corresponding to output nodes 412 and 414 are set, and the remaining storage elements are not set, after a shift left operation storage elements corresponding to output node 412, 414, and 416 are set. When shift register 330 is utilized in a variable delay line such as variable delay line 108A (Figure 3), this corresponds to a single delay cell, such as delay cell 312, being inserted in the delay path.

The shift left and shift right operations work across block boundaries. For example, if the storage element corresponding to output node 418 is set, and the storage element corresponding to output node 442 is not set, a shift left operation will set the storage element corresponding to output node 442. The state of output node 418 is input to block 440 at least significant bit input 419. When block 440 performs a left shift operation, the storage element corresponding to output node 442 receives the value at the least significant bit input 419. Shift right operations work the same way as shift left operations, with the exception that they work to the right rather than the left.

The coarse increase signal on node 474 is input to logic gates 420 and 450. Logic gate 420 combines the coarse increase signal with a most significant bit from a less significant stage on node 421. The output of logic gate 420 drives the "set all" input node 422 of block 410. The set all input node, when asserted, causes all storage elements within block 410 to be set. Likewise, logic gate 450 combines the coarse increase signal with the most significant bit from block 410 and drives the set all input node 452 of block 440. When the most significant bit of block 410 is asserted, output node 418 is also asserted. If, when output node 418 is asserted, the coarse increase

signal is also asserted, set all input node 452 of block 440 is also asserted. As a result, all storage elements within block 440 are set in one operation.

The coarse decrease signal on node 476 causes an operation similar to the coarse increase signal, but in the opposite direction. Coarse decrease signal on node 476 is input to logic gates 458 and 428. Logic gates 458 and 428 also receive the least significant bit of the more significant stage. If the coarse decrease signal is asserted when the least significant bit of the more significant stage is not set, the "reset all" input node is asserted causing the entire block of storage elements to be reset. For example, block 410 receives a signal from logic gate 428 on reset all input node 430. When the least significant bit of block 440 is not set, output node 442 is not asserted. If, when output 442 is not asserted, the coarse decrease signal on node 476 is asserted, reset all input node 430 will be asserted. This causes all storage elements within block 410 to be reset.

In the embodiment of Figure 4, a shift register can be shifted left or right by a single storage element, or can be shifted left or right by four storage elements at a time. In other embodiments, blocks hold more than four storage elements, resulting in larger coarse adjustments. In other embodiments, blocks hold less than four storage elements, resulting in smaller coarse adjustments. In still other embodiments, blocks hold varying numbers of storage elements, such that different size coarse adjustments can be made.

Figure 5 is an alternate embodiment of a variable delay line. Variable delay line 108B is one embodiment of variable delay line 108. Variable delay line 108B is divided into a coarse adjustment portion, and a fine adjustment portion. The coarse adjustment portion includes shift register 502 and coarse delay cells 532, 534, and 536. The fine adjustment portion includes shift register 512 and fine delay cells 542, 544, and 546. The coarse adjustment portion and the fine adjustment portion each function similar to variable delay line 108A (Figure 3). For example, shift register 502 receives the coarse increase signal from node 508 on shift left input node 504. Shift register 502 also receives the coarse decrease signal from node 510 on shift right input node 506. When shift register 502 receives an asserted signal on shift left input node 504, more output nodes become asserted. When shift register 502 receives an asserted signal on

the shift right input node 506, fewer output nodes are asserted. The result is a change in the number of coarse delay cells included within the clock path of variable delay line 108B.

The coarse delay cells receive E_CLOCK from node 530 and produce an intermediate clock on node 540. The intermediate clock on node 540 is received by the fine adjustment portion of variable delay line 108B. Node 540 is input to fine delay cells 542, 544, and 546. Shift register 512, in response to signals received on shift left input node 514 and shift right input node 516, increases or decreases the number of output nodes asserted. This is similar to the operation of shift register 502. After E_CLOCK travels through coarse delay cells and fine delay cells, an internal clock is generated on node 560.

Variable delay line 108B is shown with three coarse delay cells, and three fine delay cells. Any number of coarse delay cells and fine delay cells can be used without departing from the scope of the present invention.

Figure 6 shows waveforms of signals during the operation of a variable delay line. One variable delay line embodiment, the operation of which is described by Figure 6, includes phase detector 130 (Figure 2), variable delay line 108A (Figure 3), and shift register 330 (Figure 4). E_CLOCK 602 corresponds to E_CLOCK on node 202, and I_CLOCK 622 corresponds to I_CLOCK on node 204 (Figure 2). The phase of E_CLOCK 602 is compared to the phase of I_CLOCK 622 during each period of E_CLOCK 602. For example, during period 680, E_CLOCK 602 is compared to I_CLOCK 622 and phase difference 604 results. Phase difference 604 is a phase difference in which E_CLOCK 602 lags I_CLOCK 622 by more than the delay of delay line 206 (Figure 2). As a result, coarse increase signal 640 is asserted at 642. Fine increase signal 650 is also asserted at 652.

As a result of the assertions of coarse increase signal 640 and fine increase signal 650, I_CLOCK 622 is slightly retarded relative to E_CLOCK 602. When the comparison occurs again during period 682, phase difference 606 results. Phase difference 606 is still greater than the delay of delay line 206, and as a result, coarse increase signal 640 is asserted at 644, and fine increase signal 650 is asserted at 654.

I_CLOCK 622 is again delayed further as a result. During period 684 the comparison of E_CLOCK 602 and I_CLOCK 622 yields phase difference 608. Phase difference 608 is less than the delay of delay line 206, and as a result, coarse increase signal 640 is not asserted, but fine increase signal 650 is asserted at 656. During period 686 the phase comparison yields phase difference 610, which results in fine increase signal 650 being asserted at 658. Thereafter, the phase comparison yields phase offset 612 which is less than a threshold in phase comparator 220, and neither coarse increase signal 640 nor fine increase signal 650 are asserted.

In the operational scenario shown in Figure 6, E_CLOCK 602 lags I_CLOCK 622, and the delay of the variable delay line is increased until the phase of E_CLOCK 602 and I_CLOCK 622 substantially align. Coarse decrease signal 660 and fine decrease signal 670 were not used in this scenario because I_CLOCK 622 did not lag E_CLOCK 602. One skilled in the art will understand that when I_CLOCK 622 lags E_CLOCK 602, coarse decrease signal 660 and fine decrease signal 670 can be used to reduce phase offsets until E_CLOCK 602 and I_CLOCK 622 substantially align in phase.

Figure 7 shows a processing system according to the invention. System 700 includes processor 702, and memory 704. System 700 can also include many other devices such as memory controllers, input/output devices, and others. These other devices are ommitted from Figure 7 to accentuate the items remaining in the figure. Processor 702 can be a microprocessor, digital signal processor, embedded processsor, microcontroller, or the like. Memory 704 is a memory device that includes a delay lock loop such as the delay lock loop shown in Figure 1. Processor 702 and memory 704 communicate using address signals on node 708, control signals on node 710, and data signals on node 706. In some embodiments, a clock signal generated by a delay lock loop internal to memory 704 is used to drive control inputs of circuit elements that drive outputs of memory 704. For example, data signals on node 706 can be driven by circuit elements such as device element 112 (Figure 1). The delay lock loop internal to memory 704 provides a mechanism for efficient communications between processor 702 and memory 704.

Conclusion

A variable delay line and method therefor have been described. The variable delay line can be used in a delay lock loop within an integrated circuit. The variable delay line receives coarse and fine adjustment controls from phase comparators. The coarse and fine adjustment controls cause a shift register associated with the delay element to shift varying amounts, thereby causing a varying amount of delay to be added or removed from the variable delay line. In one embodiment, the shift register is grouped into blocks, and the shift register shifts a block at a time in response to the coarse controls. In another embodiment, one shift register adds or removes coarse delay cells in response to the coarse controls, and another shift register adds or removes fine delay cells in response to the fine controls.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method of operation of a delay lock loop comprising:

comparing a phase of a first clock signal with a phase of a second clock signal to generate a first control signal;

delaying the first clock signal to generate a first delayed clock signal;

comparing a phase of the first delayed clock signal with the phase of the second clock signal to generate a second control signal; and

shifting a phase of the first clock signal in response to the first control signal and the second control signal.

2. The method of claim 1 wherein shifting comprises:

responsive to the first control signal, shifting the phase of the first clock signal by a first amount; and

responsive to the second control signal, shifting the phase of the first clock signal by a second amount, wherein the second amount is greater than the first amount.

3. The method of claim 1 further comprising:

delaying the second clock signal to generate a second delayed clock signal;

comparing a phase of the second delayed clock signal with the phase of the first clock signal; and

shifting the phase of the first clock signal a third amount in response to the third control signal.

4. The method of claim 3 wherein the third amount is substantially equal to the second amount.

5. A method of setting a delay value in a delay lock loop comprising:

delaying a first signal in a variable delay line to generate a second signal;

comparing a phase of the first signal with a phase of the second signal to generate a first control signal;

delaying the first signal by a first substantially fixed amount to generate a third signal;

comparing the phase of the second signal with a phase of the third signal to generate a second control signal;

responsive to the first control signal, adjusting the variable delay line by a first delay amount; and

responsive to the second control signal, adjusting the variable delay line by a second delay amount, the second delay amount being greater than the first delay amount.

6. The method of claim 5 further comprising:

delaying the second signal by a second substantially fixed amount to generate a fourth signal;

comparing the phase of the first signal with a phase of the fourth signal to generate a third control signal; and

responsive to the third control signal, adjusting the variable delay line by a third delay amount.

7. The method of claim 6 wherein the second delay amount and the third delay amount are substantially equal.

8. The method of claim 6 wherein the first substantially fixed amount and the second substantially fixed amount are substantially equal.

9. The method of claim 6 wherein the first delay amount and the second delay amount are opposite in polarity.

10. A method of aligning the phase of a first signal external to a device and the phase of a second signal internal to the device comprising:

receiving the first signal into the device, and subjecting the first signal to a device boundary delay to produce an internal first signal;

delaying the internal first signal in a variable delay line to generate the second signal, the variable delay line having a fine adjustment control and a coarse adjustment control;

delaying the second signal a substantially fixed amount to produce a delayed second signal;

comparing the internal first signal with the second signal, and responsive thereto, driving the fine adjustment control; and

comparing the internal first signal with the delayed second signal, and responsive thereto, driving the coarse adjustment control.

11. The method of claim 10 wherein prior to delaying the second signal or comparing the internal first signal with the second signal, the method further comprises subjecting the second signal to an additional delay substantially equal to the device boundary delay.

12. The method of claim 10 wherein the variable delay line has a second coarse adjustment control and the method further comprises:

delaying the internal first signal the substantially fixed amount to produce a delayed internal first signal; and

comparing the delayed internal first signal and the second signal, and responsive thereto, driving the second coarse adjustment.

13. The method of claim 12 wherein the first coarse adjustment and the second coarse adjustment result in adjustments of opposite polarity.

14. In a memory device having data output drivers configured to drive data signals external to the memory device, a method of aligning the data signals with an external clock signal comprising:

receiving the external clock signal;

delaying the external clock signal in a variable delay line having a variable delay associated therewith, to produce an internal clock signal;

generating a phase difference between the external clock signal and the internal clock signal;

comparing the phase difference to a threshold;

when the phase difference is above the threshold, changing the variable delay a first delay amount;

when the phase difference is not above the threshold, changing the variable delay a second delay amount, the second delay amount being less than the first delay amount; and

driving a control input of the data output drivers with the internal clock.

15. The method of claim 14 wherein the data output drivers are sequential devices having clock inputs, and driving a control input comprises driving the clock inputs of the sequential devices.

16. The method of claim 14 wherein the data output drivers are devices having output enable inputs, and driving a control input comprises driving the output enable inputs of the data output drivers.

17. The method of claim 14 wherein generating a phase difference and comparing the phase difference comprise:

delaying the internal clock signal by an amount substantially equal to the threshold to generate a delayed internal clock signal; and

comparing the delayed internal clock signal to the external clock signal.

18. The method of claim 14 wherein generating a phase difference and comparing the phase difference comprise:

delaying the external clock signal by an amount substantially equal to the threshold to generate a delayed external clock signal; and

comparing the delayed external clock signal to the internal clock signal.

19. The method of claim 14 wherein the external clock signal has a period associated therewith, and the variable delay line delays the external clock signal such that the internal clock signal lags the external clock signal by an integer number of periods.

20. In a delay line having a variable delay, a method of changing the variable delay comprising:

comparing a phase of a signal input to the delay line with a phase of a signal output from the delay line to produce a phase difference;

when the phase difference is larger than a first threshold, adjusting the variable delay by a first delay amount; and

when the phase difference is not larger than the first threshold and is larger than a second threshold, adjusting the variable delay by a second delay amount, the second delay amount being less than the first delay amount.

21. The method of claim 20 further comprising:

responsive to the comparing, when the phase difference is smaller than the second threshold, holding the variable delay constant.

22. The method of claim 20 wherein the delay line comprises a plurality of delay elements, each of the plurality of delay elements having a unit delay, and wherein the second delay amount is substantially equal to one unit delay.

23. The method of claim 22 wherein the first delay amount is substantially equal to an integer number of unit delays.

24. A phase detector comprising:

a first input node, a second input node, a first output node, and a second output node;

a first phase comparator coupled between the first input node, the second input node, and the first output node;

a first delay line coupled to the first input node; and

a second phase comparator coupled between the first delay line, the second input node, and the second output node.

25. The phase detector of claim 24 further comprising:

a third output node;

a second delay line coupled to the second input node; and

a third phase comparator coupled between the first input node, the second delay line, and the third output node.

26. The phase detector of claim 24 wherein the first phase comparator is configured to produce at least one fine delay line adjustment control, and the second phase comparator is configured to produce at least one coarse delay line adjustment control.

27. A delay lock loop comprising:

a variable delay line including a plurality of delay cells;

a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift register having a fine control input node, and a course control input node; and

a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node.

28. The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of storage elements in response to an asserted signal on the fine control input node.

29. The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.

30. The delay lock loop of claim 27 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.

31. The delay lock loop of claim 30 wherein the phase detector is configured to assert a coarse control signal on the coarse adjustment output node when the phase difference is above a threshold, and to assert a fine control signal on the fine adjustment output node when the phase difference is below the threshold.

32. The delay lock loop of claim 27 wherein the plurality of delay cells each exhibit substantially the same delay.

33. The delay lock loop of claim 27 wherein the plurality of delay cells do not all exhibit the same delay.

34. A variable delay line comprising:

a coarse adjustment portion comprising a first plurality of delay cells and a first shift register; and

a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells.

35. The variable delay line of claim 34 wherein the first shift register is configured to be responsive to coarse adjustment signals from a phase detector.

36. The variable delay line of claim 34 wherein the second shift register is configured to be responsive to fine adjustment signals from a phase detector.

37. An integrated circuit comprising:

a variable delay line having an input node, an output node, a fine adjustment input node, and a coarse adjustment input node; and

a phase detector configured to compare a signal on the input node with a signal on the output node and drive signals onto the fine adjustment input node and the coarse adjustment input node.

38. The integrated circuit of claim 37 wherein the fine adjustment input node comprises:

a fine increase adjustment input node; and

a fine decrease adjustment input node.

39. The integrated circuit of claim 37 wherein the coarse adjustment input node comprises:

a coarse increase adjustment input node; and

a coarse decrease adjustment input node.

40. The integrated circuit of claim 37 further comprising an output driver responsive to the signal on the output node of the variable delay line.

41. The integrated circuit of claim 37 wherein the output driver is a synchronous element having a clock input node, and the clock input node is coupled to the output node of the variable delay line.

42. The integrated circuit of claim 37 wherein the output driver includes an output enable input node coupled to the output node of the variable delay line.

43. The integrated circuit of claim 37 wherein the integrated circuit is a memory device.

44. The integrated circuit of claim 37 wherein the integrated circuit is an application specific integrated circuit.

45. The integrated circuit of claim 37 wherein the integrated circuit is a processor.

46. A processing system comprising:

a processor; and

a memory having a delay lock loop comprising:

a variable delay line including a plurality of delay cells;

a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift register having a fine control input node, and a course control input node; and

a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node.

47. The processing system of claim 46 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.

48. The processing system of claim 46 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.

49. A processing system comprising:

a processor; and

a memory having a delay lock loop that includes a phase detector comprising:

a first input node, a second input node, a first output node, and a second output node;

a first phase comparator coupled between the first input node, the second input node, and the first output node;

a first delay line coupled to the first input node; and

a second phase comparator coupled between the first delay line, the second input node, and the second output node.

50. The processing system of claim 49 wherein the phase detector further comprises:

a third output node;

a second delay line coupled to the second input node; and

a third phase comparator coupled between the first input node, the second delay line, and the third output node.

51. A processing system comprising:

a processor; and

a memory having a delay lock loop that includes a variable delay line comprising:

a coarse adjustment portion comprising a first plurality of delay cells and a first shift register; and

a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells.

52. The processing system of claim 51 wherein the first shift register is configured to be responsive to coarse adjustment signals from a phase detector.

53. The processing system of claim 52 wherein the second shift register is configured to be responsive to fine adjustment signals from a phase detector.

Abstract of the Disclosure

A variable delay line includes a shift register responsive to coarse adjustment control and a fine adjustment control. The variable delay line can be used in a delay lock loop within an integrated circuit. The variable delay line receives coarse and fine adjustment controls from phase comparators within a phase detector. The coarse and fine adjustment controls cause a shift register associated with the delay element to shift varying amounts, thereby causing a varying amount of delay to be added or removed from the variable delay line. The shift register can be grouped into blocks, and the shift register can shift a block at a time in response to the coarse controls. The variable delay line can also include coarse delay cells associated with one shift register and fine delay cells associated with another shift register. One shift register adds or removes coarse delay cells in response to the coarse controls, the other shift register adds or removes fine delay cells in response to the fine controls.

"Express Mail" mailing label number: EL517792640US

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Printed Name: Shawn Hise

Signature:

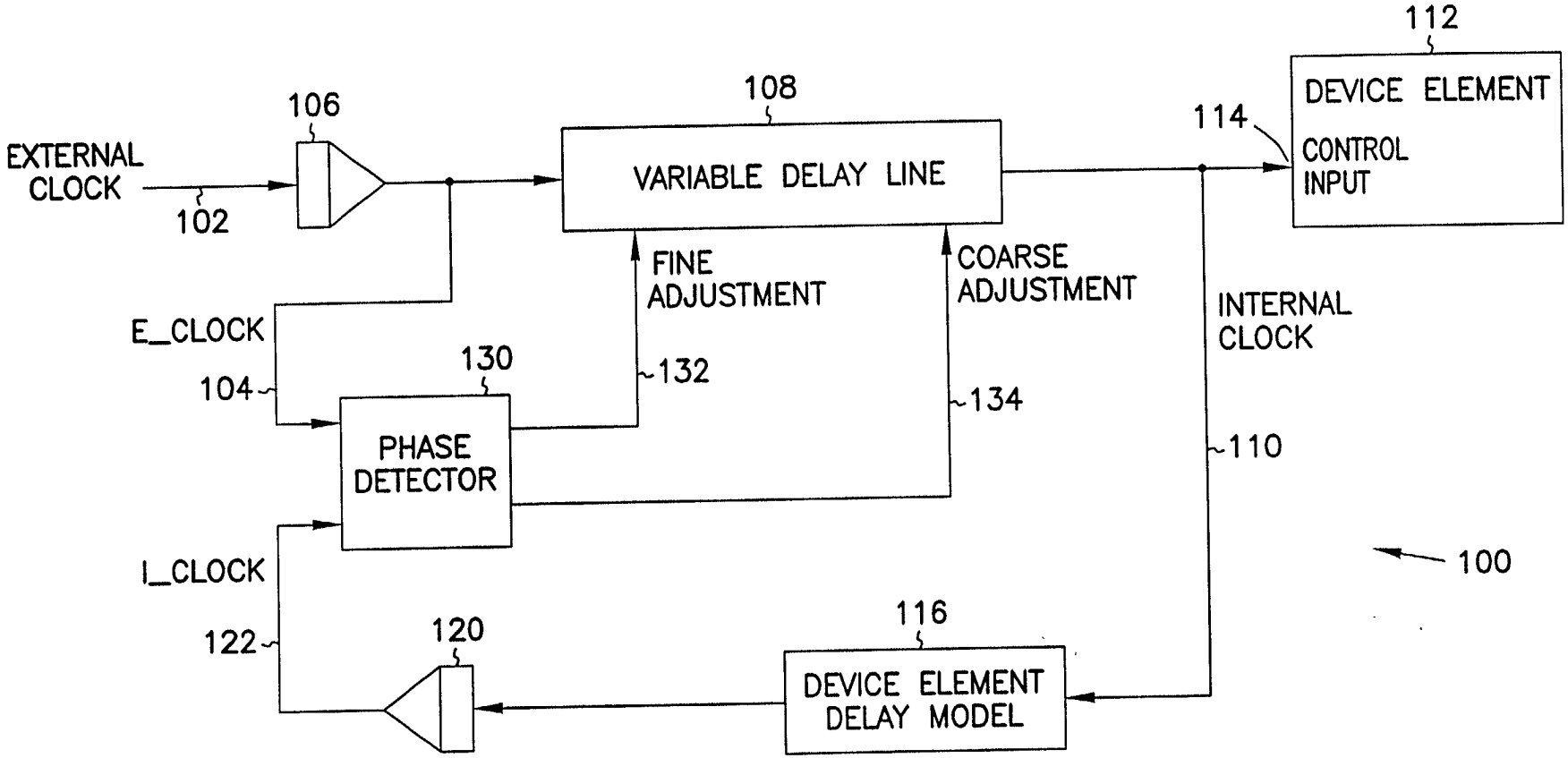
112
DEVICE ELEMENT
CONTROL INPUT
114
108
VARIABLE DELAY LINE
106
EXTERNAL CLOCK
102
FINE ADJUSTMENT
COARSE ADJUSTMENT
INTERNAL CLOCK
E_CLOCK
104
130
PHASE DETECTOR
132
134
110
100
I_CLOCK
122
120
116
DEVICE ELEMENT DELAY MODEL

FIG. 1

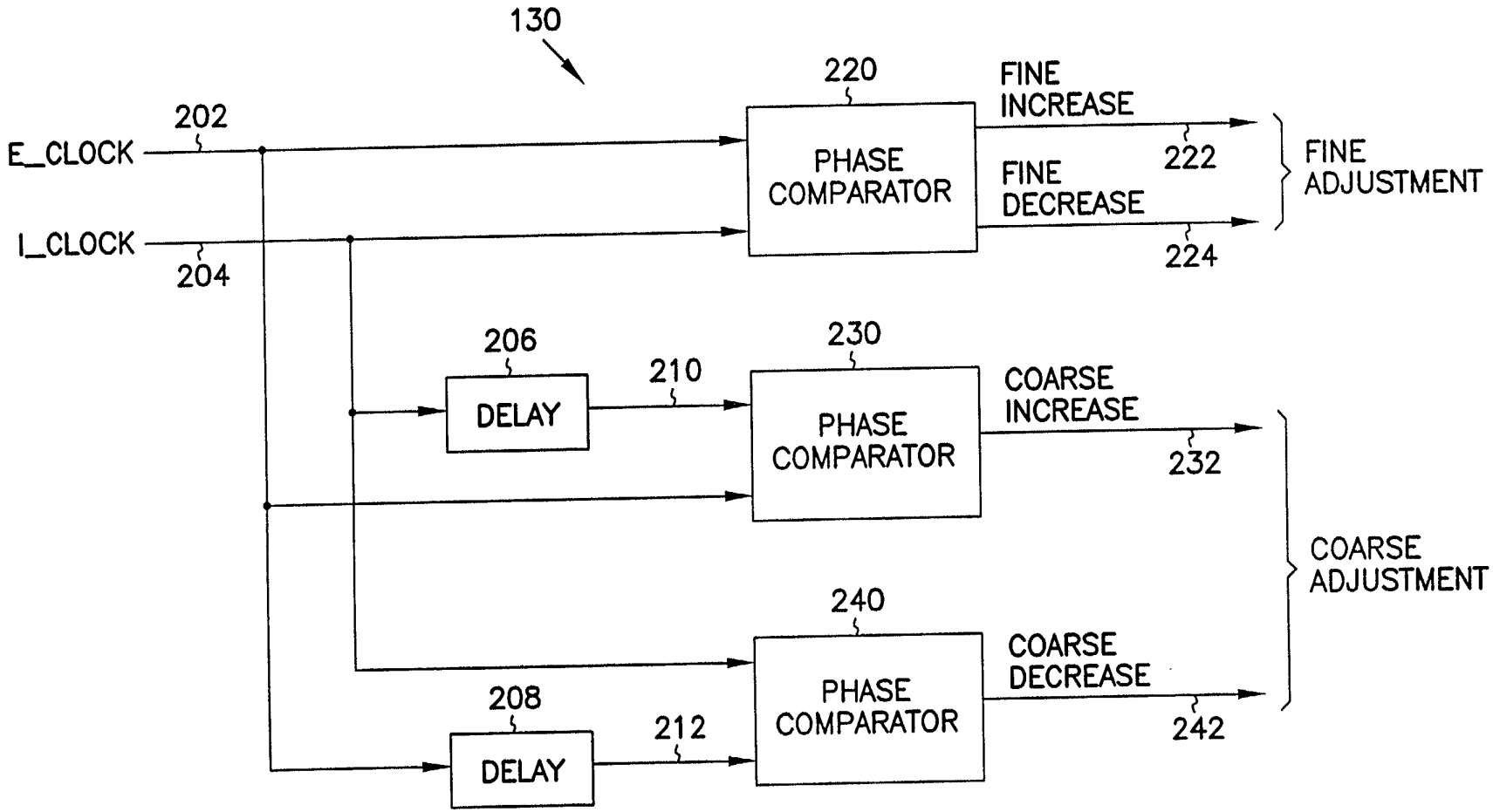
130
220
FINE
INCREASE
202
E_CLOCK
PHASE
COMPARATOR
222
FINE
ADJUSTMENT
FINE
DECREASE
I_CLOCK
204
224
206
230
210
DELAY
COARSE
INCREASE
PHASE
COMPARATOR
232
COARSE
ADJUSTMENT
240
COARSE
DECREASE
208
PHASE
COMPARATOR
212
DELAY
242

FIG. 2

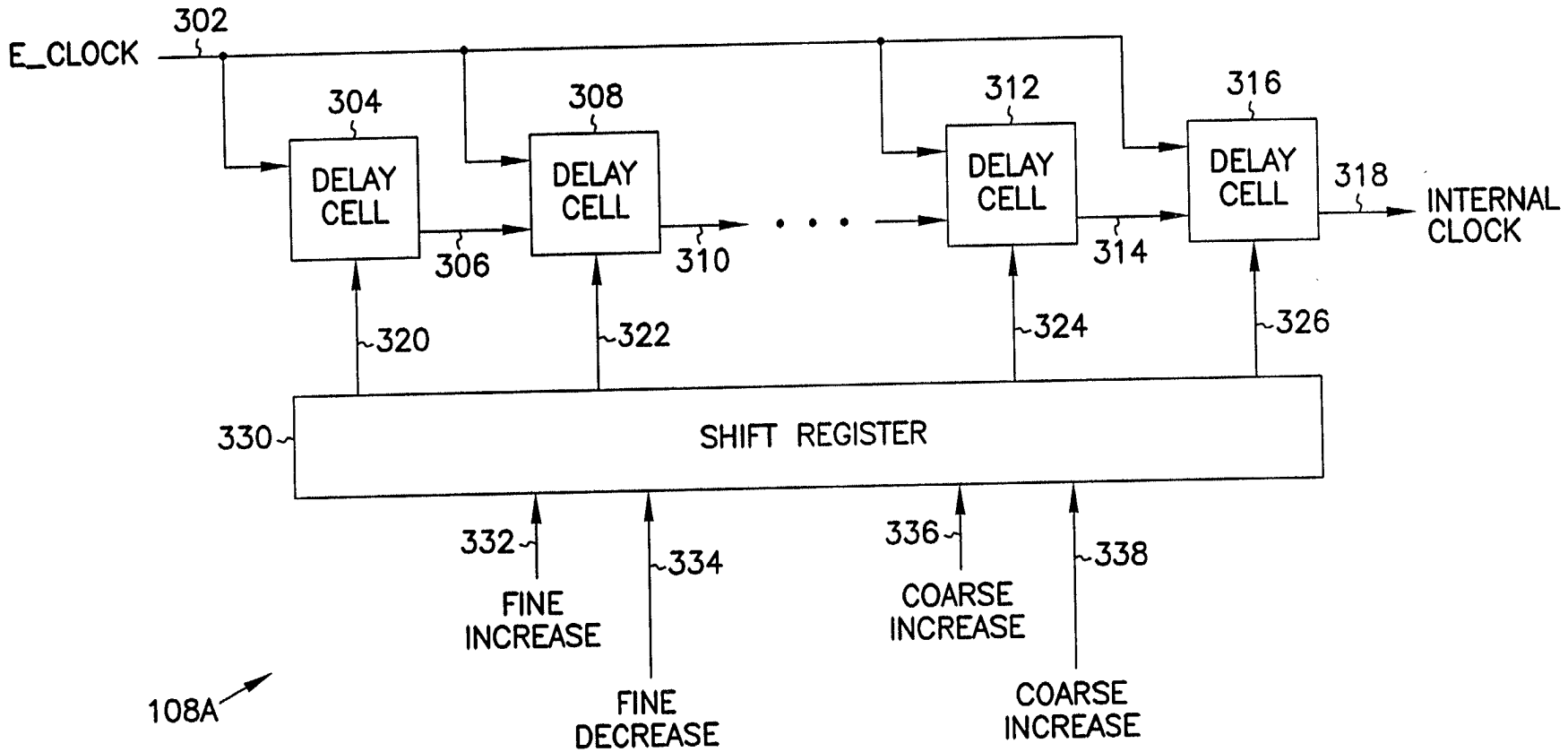
E_CLOCK
302
304
308
312
316
DELAY CELL
DELAY CELL
DELAY CELL
DELAY CELL
318
INTERNAL CLOCK
306
310
314
320
322
324
326
330
SHIFT REGISTER
332
334
336
338
FINE INCREASE
FINE DECREASE
COARSE INCREASE
COARSE INCREASE
108A

FIG. 3

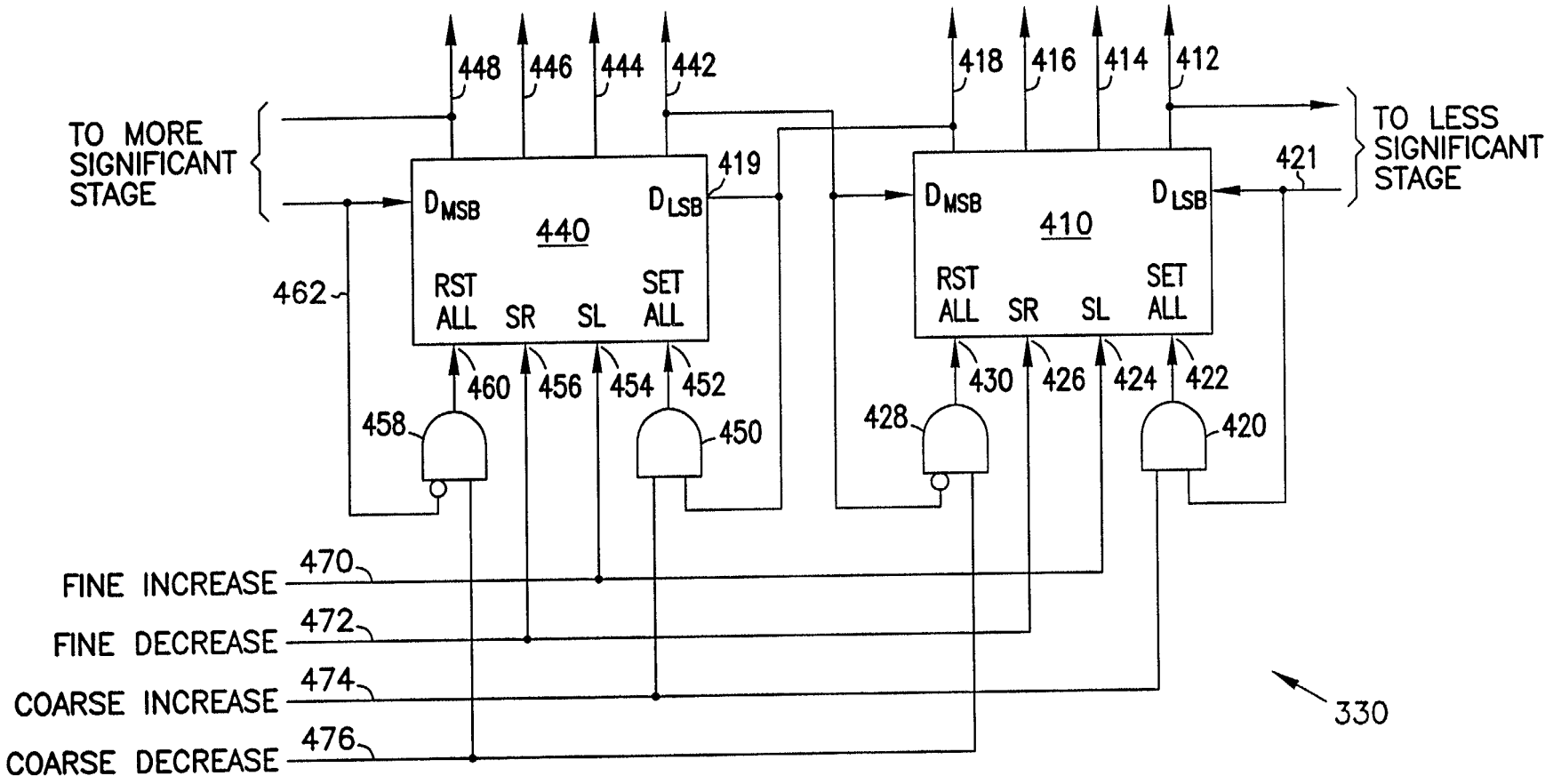
TO MORE SIGNIFICANT STAGE
448
446
444
442
419
D_{MSB}
D_{LSB}
440
RST ALL
SR
SL
SET ALL
462
460
456
454
452
458
450
418
416
414
412
421
TO LESS SIGNIFICANT STAGE
410
430
426
424
422
428
420
FINE INCREASE
470
FINE DECREASE
472
COARSE INCREASE
474
COARSE DECREASE
476
330

FIG. 4

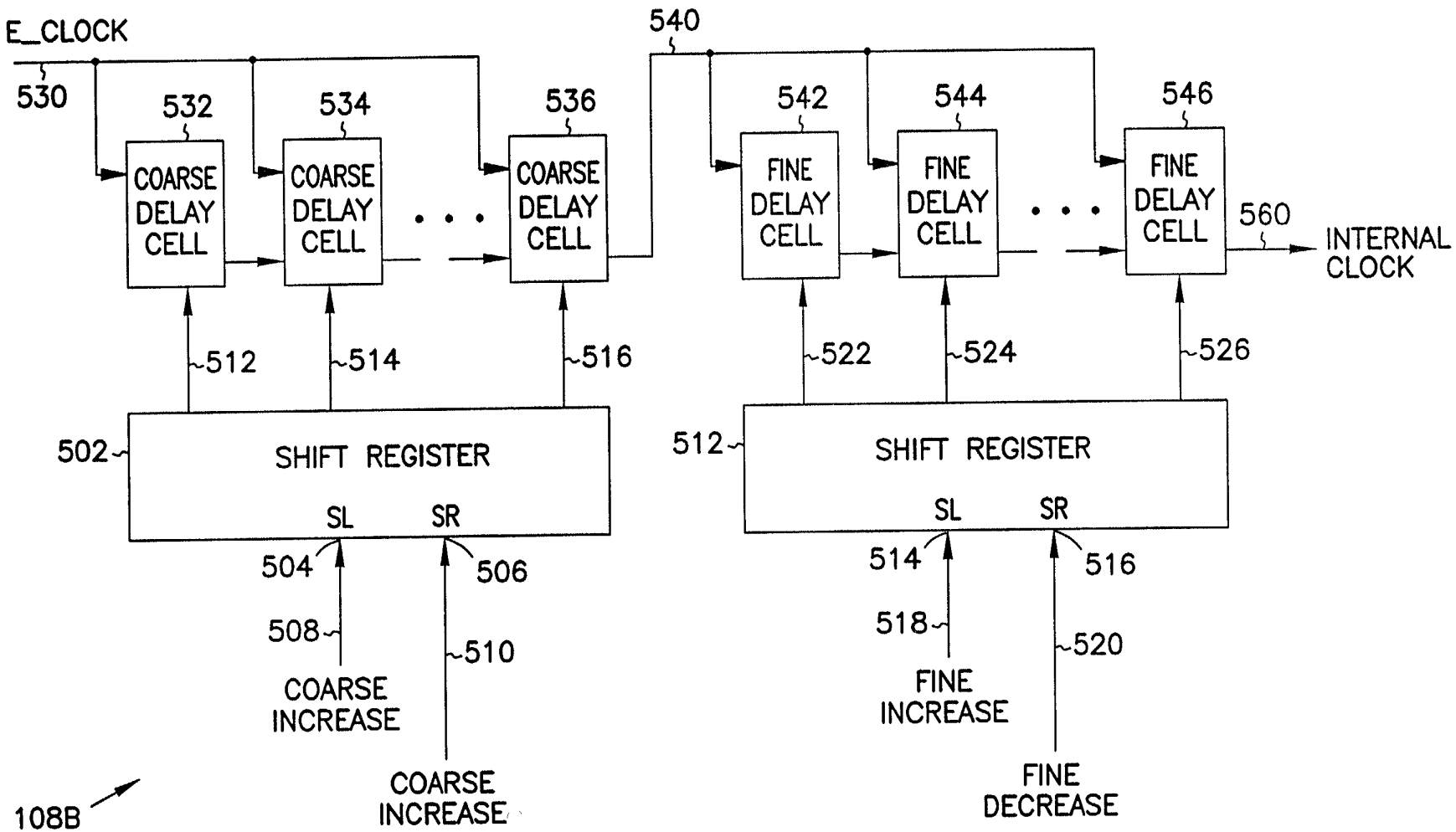
E_CLOCK
530
532
534
536
540
542
544
546
COARSE DELAY CELL
COARSE DELAY CELL
COARSE DELAY CELL
FINE DELAY CELL
FINE DELAY CELL
FINE DELAY CELL
560
INTERNAL CLOCK
512
514
516
522
524
526
502
SHIFT REGISTER
SL
SR
504
506
508
510
COARSE INCREASE
COARSE INCREASE
512
SHIFT REGISTER
SL
SR
514
516
518
520
FINE INCREASE
FINE DECREASE
108B

FIG. 5

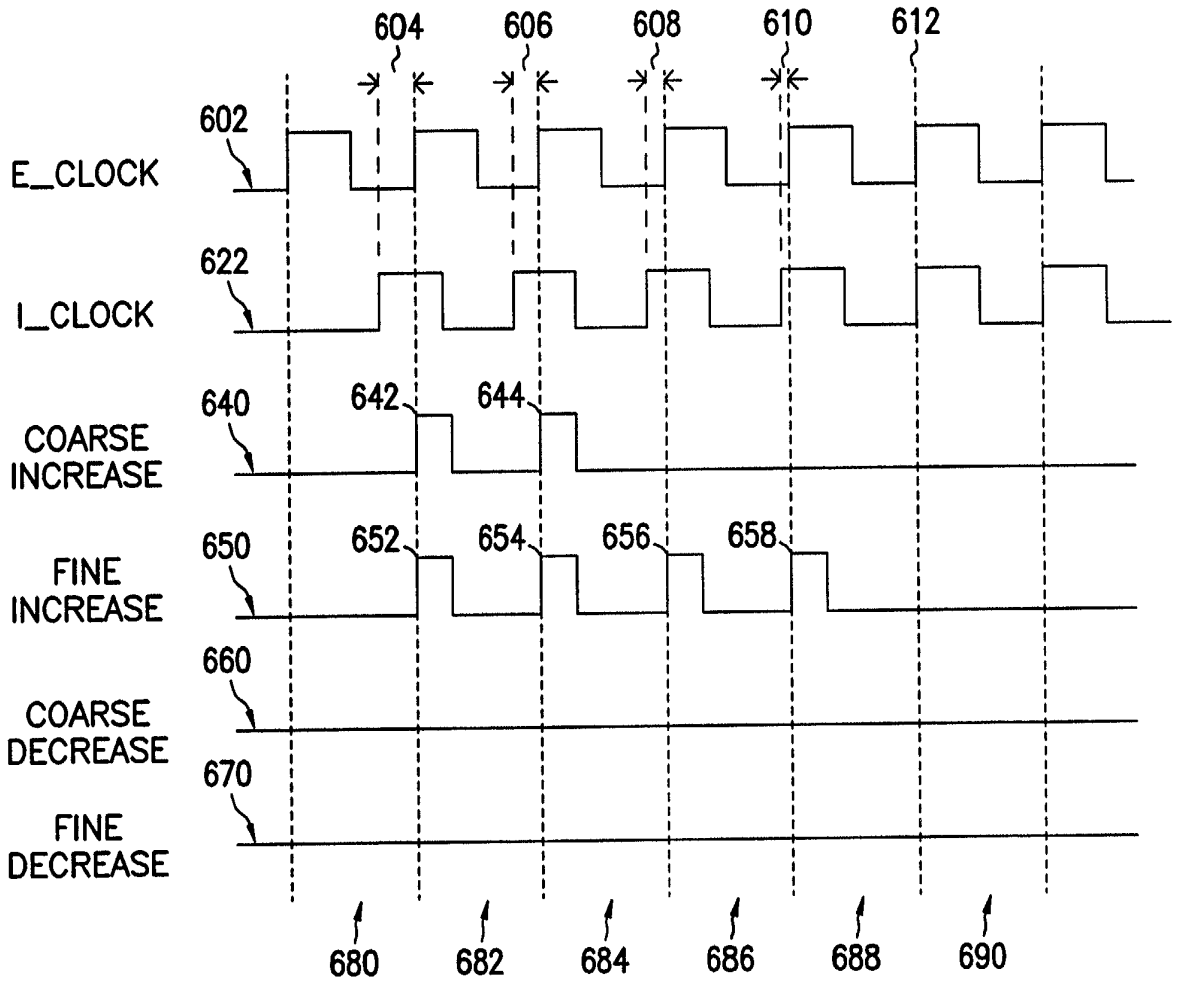
604
606
608
610
612
602
E_CLOCK
622
I_CLOCK
640
642
644
COARSE INCREASE
650
652
654
656
658
FINE INCREASE
660
COARSE DECREASE
670
FINE DECREASE
680
682
684
686
688
690

FIG. 6

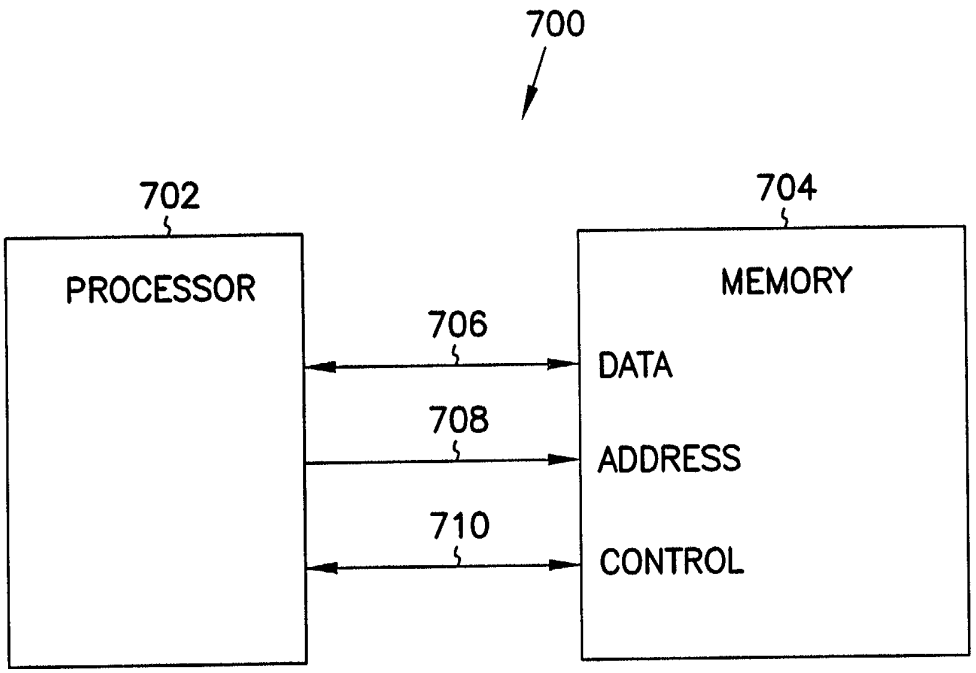
700
702
PROCESSOR
704
MEMORY
706
DATA
708
ADDRESS
710
CONTROL

FIG. 7

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

VARIABLE DELAY LINE .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship: **United States of America** Residence: **Boise, ID**
Post Office Address: 4488 S. Tableridge Way
Boise, ID 83705

Signature: _____ Date: 1/12/00
Eric T. Stubbs

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Eric T. Stubbs	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.662US1	
Title:	VARIABLE DELAY LINE		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Gregory J.	Reg. No. 44,494	Huebsch, Joseph C.	Reg. No. 42,673	Nielsen, Walter W.	Reg. No. 25,539
Anglin, J. Michael	Reg. No. 24,916	Jurkovich, Patti J.	Reg. No. 44,813	Oh, Allen J.	Reg. No. 42,047
Bentley, Dwayne L.	Reg. No. P-45,947	Kalis, Janal M.	Reg. No. 37,650	Padys, Danny J.	Reg. No. 35,635
Bianchi, Timothy E.	Reg. No. 39,610	Kaufmann, John D.	Reg. No. 24,017	Parker, J. Kevin	Reg. No. 33,024
Billion, Richard E.	Reg. No. 32,836	Klima-Silberg, Catherine I.	Reg. No. 40,052	Peacock, Gregg A.	Reg. No. 45,001
Black, David W.	Reg. No. 42,331	Kluth, Daniel J.	Reg. No. 32,146	Perdok, Monique M.	Reg. No. 42,989
Brennan, Leoniede M.	Reg. No. 35,832	Lacy, Rodney L.	Reg. No. 41,136	Polglaze, Daniel J.	Reg. No. 39,801
Brennan, Thomas F.	Reg. No. 35,075	Leffert, Thomas W	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Brooks, Edward J., III	Reg. No. 40,925	Lemaire, Charles A.	Reg. No. 36,198	Schumm, Sherry W.	Reg. No. 39,422
Chu, Dinh C.P.	Reg. No. 41,676	Litman, Mark A.	Reg. No. 26,390	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Lundberg, Steven W.	Reg. No. 30,568	Shaw, Stephen H.	Reg. No. P-45,404
Dahl, John M.	Reg. No. 44,639	Mack, Lisa K.	Reg. No. 42,825	Slifer, Russell D.	Reg. No. 39,838
Drake, Eduardo E.	Reg. No. 40,594	Maki, Peter C.	Reg. No. 42,832	Smith, Michael G.	Reg. No. P-45,368
Eliseeva, Maria M.	Reg. No. 43,328	Malen, Peter L.	Reg. No. 44,894	Speier, Gary J.	Reg. No. P-45,458
Embretson, Janet E.	Reg. No. 39,665	Mates, Robert E.	Reg. No. 35,271	Steffey, Charles E.	Reg. No. 25,179
Fogg, David N.	Reg. No. 35,138	McCrackin, Ann M.	Reg. No. 42,858	Terry, Kathleen R.	Reg. No. 31,884
Fordenbacher, Paul J.	Reg. No. 42,546	Nama, Kash	Reg. No. 44,255	Viksnins, Ann S.	Reg. No. 37,748
Forrest, Bradley A.	Reg. No. 30,837	Nelson, Albin J.	Reg. No. 28,650	Woessner, Warren D.	Reg. No. 30,440
Harris, Robert J.	Reg. No. 37,346				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Attn: Daniel J. Kluth
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 373-6904
Facsimile: (612) 339-3061

Dated: 1-26-00

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel